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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/550,598

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Hee-Seob Kim

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EXAMINER

CALEY, MICHAEL H

ART UNIT

PAPER NUMBER

2871

NOTIFICATION DATE

DELIVERY MODE

03/18/2010

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

usptopatentmail@cantorcolburn.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/550,598	<b>Applicant(s)</b> KIM ET AL.	
	<b>Examiner</b> MICHAEL H. CALEY	<b>Art Unit</b> 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 November 2009.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-13 is/are allowed.
- 6) ☒ Claim(s) 1-7 and 14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 September 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)                        | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Examination Notes***

Page 7 of Remarks indicates a certified English translation of the priority document as filed with the 11/30/09 reply, however, there is no record of the certified translation as having been filed.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**Claims 1-7 and 14 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 line 10 references “the first pixel electrode”, which lacks antecedent basis. It is unclear whether this reference is intended to refer to the “first electrode” or a separate “first pixel electrode”. For examination on the merits, it is assumed that “the first pixel electrode” of line 10 is intended to read “the first electrode”.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 1-5 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by**

**Yamamoto et al. (U.S. Patent Application Publication No. 2002/0089813 “Yamamoto”).**

Regarding claim 1, Yamamoto discloses a thin film transistor array panel comprising:

- an insulating substrate (abstract);

- a plurality of gate lines (Figure 8 elements G1n, G2n, G1n+1) formed on the insulating substrate;

- a plurality of storage electrode lines (Bn, 66) formed on the first insulating substrate;

- a plurality of data lines (Sn, Sn+1) insulated from the gate lines; and

- a plurality of pixel areas arranged in a matrix (Figure 7), one of the pixel areas comprising:

- a first electrode (9, 12; Paragraphs [0053], [0090]) and a second electrode (26) disposed on the pixel area;

- a third electrode (22) connected to the first pixel electrode (Figure 7; note 12 and 22 are electrically connected, also note that Applicant’s specification defines a capacitive coupling as a coupling, or connection, e.g. Page 5 lines 15-17);

- a first thin film transistor (30) connected to the first electrode; and

- a second thin film transistor (40 or 50) connected to or capacitively coupled to the second electrode;

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wherein a portion of the third electrode extends parallel to one of the data lines and partially overlaps the storage electrode line (Figure 8).

Regarding claim 2, Yamamoto discloses the storage electrode line as overlapping an edge of one of the first electrode and the second electrodes (Figure 8).

Regarding claim 3, Yamamoto discloses the third electrode as connected to a drain electrode of the first thin film transistor (Figure 7).

Regarding claim 4, Yamamoto discloses the second thin film transistor as connected to one of the storage electrode lines and the data lines (Figure 8).

Regarding claim 5, Yamamoto discloses the second thin film transistor (50) as connected to one of the storage electrode lines, and one of the pixel areas further comprises a third thin film transistor (40) connected to one of the data lines, the second electrode, and one of the gate lines connected to the second thin film transistor (Figure 8).

Regarding claim 7, Yamamoto discloses a gate insulating layer (Paragraph [0045]) disposed between the gate lines and the data lines; and a passivation layer (Paragraph [0053]) disposed between the data lines and the first and the second electrodes, wherein the third electrode is connected to the first electrode through a contact hole at the passivation layer (Paragraph [0053]).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Kim et al. (U.S. Patent No. 6,473,142 “Kim”).**

Yamamoto fails to disclose at least one of the pixel electrodes as having at least one domain partitioning member. Kim, however, teaches a domain partitioning member on a pixel electrode (element 57) as a means of creating a multi-domain display characteristic (Column 2 lines 1-4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a domain partitioning member on at least one of the pixel electrodes. One would have been motivated to form such a domain partitioning member as a means of improving brightness and image stability at wide viewing angles (Column 2 lines 1-4).

**Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Mimura et al. (U.S. Patent No. 5,283,566 “Mimura”).**

Yamamoto fails to disclose two storage lines as connected to each other through a storage bridge. Mimura, however, teaches a storage bridge (Figure 1 element 9) for maintaining the storage electrode at a same fixed potential (Column 3 lines 12-16).

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It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a storage bridge connecting storage electrode lines as proposed. One would have been motivated to form the storage bridge as a means of maintaining the fixed potential among storage lines to maximize the storage capacitance function according to conventional means (Mimura: Column 3 lines 12-16).

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-7 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claims 8-13 have been fully considered and are persuasive. The rejection of claims 8-13 has been withdrawn.

### ***Allowable Subject Matter***

Claims 8-13 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Amendment and arguments filed on 11/30/09 are persuasive in identifying that Song and Hiraishi fail to disclose a portion of the coupling electrode as extending parallel to one of the data lines and partially overlapping the storage electrode line (Remarks, Pages 6-7).

### ***Conclusion***

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL H. CALEY whose telephone number is (571)272-2286. The examiner can normally be reached on M-F 6:00 a.m - 2:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael H. Caley/  
Primary Examiner, Art Unit 2871